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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,214	08/27/2003	Masaru Numano	242056US2	4336

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EXAMINER	
VANNUCCI, JAMES	
ART UNIT	**PAPER NUMBER**
2828	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,214	NUMANO, MASARU	
	Examiner	Art Unit	
	Jim Vannucci	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-14 and 16-20* is/are rejected.

7)☒ Claim(s) *3 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8-27-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 7-8, 11-14 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshilawa(4,745,610) in view of Cooper et al.(6,078,204).

Claims 1 and 13, figure 6 of Yoshilawa discloses an optical semiconductor element(51) that is a load attached to circuitry containing zener diodes(41 & 42).

Alderman does not disclose the recited circuitry.

Figures 4 and 6 of Cooper disclose a circuit(90) connected to a load(18) having a series rectifying circuit including a plurality of zener diodes(34, 36 & 38) connected in series, and a rectifying element(66) whose anode is connected to an anode of the series rectifying circuit. The circuitry disclosed in Cooper protects the load(abstract).

Claims 2 and 14, the circuit disclosed in Cooper includes a voltage supply(20) which supplies a higher voltage to a cathode of the series rectifying circuit than to a cathode of the rectifying element.

Claim 7, if the optical semiconductor element disclosed in Yoshilawa is used as the load disclosed in Cooper, it would be protected from a voltage exceeding a predetermined value by a breakdown of the zener diodes.

Claims 8 and 20, the voltage that is applied to the load disclosed in Cooper is adjusted by a breakdown of the zener diodes when a voltage exceeding a predetermined value is applied.

Claims 11 and 18, the optical semiconductor element(51) disclosed in figure 9 of Yoshilawa is a light emitting element.

Claims 12 and 19, figure 9 of Yoshilawa also discloses an optical semiconductor element that is a light receiving element(61).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the zener diode circuit disclosed in Cooper with the semiconductor element load disclosed in Yoshilawa to protect the semiconductor element load as disclosed in Cooper.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa in view of Cooper as applied above, and further in view of Palara(5,521,414) and Hastings(6,617,906).

Yoshikawa and Cooper do not disclose short circuited NPN or PNT transistors.

Claims 5-6, Palara discloses that a rectifying element can be a NPN transistor(col. 4, line 22). Figure 4 of Hastings discloses a transistor(M3) whose collector and base are short-circuited.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the transistor type and connections disclosed in Hastings and Palara with the device disclosed in Yoshikawa and Cooper for improved limiting of high

voltages as disclosed in Hastings.

4. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa in view of Cooper as applied above, and further in view of Palara and Edwards et al.(4,975,798).

Yoshikawa and Cooper do not disclose short circuited NPN or PNT transistors.

Claims 5-6, Palara discloses that a rectifying element can be a NPN or PNP transistor(col. 4, line 22). Figure 2 of Edwards discloses a transistor(Q11) whose collector and base are short-circuited.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the transistor type and connections disclosed in Edwards and Palara with the device disclosed in Yoshikawa and Cooper for improved limiting of high voltages.

5. Claims 9-10 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa in view of Cooper as applied above, and further in view of Palara.

Claims 9 and 16, figure 1 of Palara discloses placing all semiconductor and circuit elements monolithically on the same semiconductor substrate.

Claims 10 and 17, the semiconductor and circuit elements disclosed in figure 1 of Palara can be accommodated in a same package.

It would have been obvious to one of ordinary skill in the art at the time of the

invention to form the elements disclosed in Yoshikawa and Cooper on a single substrate in a same package so that they will take up less space as disclosed in Palara.

Allowable Subject Matter

6. Claims 3 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter. The following limitations are primarily responsible for distinguishing these claims over the prior art.

Regarding claims 3 and 15, the limitations concerning the zener diodes having parasitic components that generate a current upon irradiation of a light thereto.

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Jim Vannucci whose phone number is (571) 272-1820.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center whose telephone number is (703) 308-0956.

Papers related to Technology Center 2800 applications only may be submitted to Technology Center 2800 by facsimile transmission. Any transmission not to be considered an official response must be clearly marked "DRAFT". The faxing of such

papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center Fax Center number is (703) 872-9306.

James Vannucci